Amendments to the Claims

Please amend claims 1, 12 and 23 as follows without acquiescence in any pending rejection or objection, or with prejudice to pursue in a related application.

1. (Currently Amended) A method of improving a design of an electronic circuit, comprising:

generating an electronic design;

automatically specifying one or more pipeline locations of the electronic design;

determining whether to insert one or more clocked elements at the one or more automatically-specified pipeline locations ~~where it is possible to insert the clocked element,~~ where a determination is ~~can be~~ made of whether to avoid inserting one or more clocked elements ~~pipelining~~ for at least one of the one or more pipeline locations; and

based upon results of determining whether to insert the one or more clocked elements, automatically modifying a number of clocked elements in the one or more pipeline locations of the design.

2. (Previously Presented) The method of claim 1, further comprising:

organizing signals in the electronic design into groups; and

specifying rules for pipelining each signal group.

3-5. (Cancelled).

6. (Previously Presented) The method of claim 1, wherein the clocked element modification is based on one or more parameters of the design addressed by the clocked element modification.

7. (Previously Presented) The method of claim 1, further comprising determining one or more placement locations for one or more of the clocked elements.

8-11. (Cancelled).

12. (Currently Amended) An apparatus for improving a design of an electronic circuit comprising:

means for generating an electronic design;

means for automatically specifying one or more pipeline locations of the electronic design;

means for determining whether to insert one or more clocked elements at the one or more automatically-specified pipeline locations ~~where it is possible to insert the clocked element,~~ where a determination is ~~can be~~ made of whether to avoid inserting one or more clocked elements ~~pipelining~~ for at least one of the one or more pipeline locations; and

means for automatically modifying a number of clocked elements in the one or more pipeline locations of the design based upon results of determining whether to insert the one or more clocked elements.

13. (Previously Presented) The apparatus of claim 12, further comprising:

means for organizing signals in the electronic design into groups; and

means for specifying rules for pipelining each signal group.

14-16. (Cancelled).

17. (Previously Presented) The apparatus of claim 12, wherein the clocked element modification is based on one or more parameters of the design addressed by the clocked element modification.

18. (Previously Presented) The apparatus of claim 12, further comprising means for determining one or more placement locations for one or more of the clocked elements.

19-22. (Cancelled).

23. (Currently Amended) An article of manufacture comprising a computer readable medium storing a computer software program which, when executed by a

computer processing system, causes the system to perform a method of improving a design of an electronic circuit, the method comprising:

automatically specifying ~~receiving~~ one or more ~~specified~~ pipeline locations of the electronic design;

determining whether to insert one or more clocked elements at the one or more automatically-specified pipeline locations ~~where it is possible to insert the clocked element,~~ where a determination is ~~can be~~ made of whether to avoid inserting one or more clocked elements ~~pipelining~~ for at least one of the one or more pipeline locations; and

based upon results of determining whether to insert the one or more clocked elements, automatically modifying a number of clocked elements in the one or more pipeline locations of the design.

24. (Previously Presented) The article of manufacture of claim 23, wherein the method further comprises:

organizing signals in the electronic design into groups; and

specifying rules for pipelining each signal group.

25-27. (Cancelled).

28. (Previously Presented) The article of manufacture of claim 23, wherein the clocked element modification is based on one or more parameters of the design addressed by the clocked element modification.

29. (Previously Presented) The article of manufacture of claim 23, wherein the method further comprises determining one or more placement locations for one or more of the clocked elements.

30-33. (Cancelled).

34. (Previously Presented) The method of claim 1, wherein the design comprises a central processing unit (CPU) in which the one or more pipeline locations are specified.

35. (Previously Presented) The method of claim 1, wherein the one or more pipeline locations are manually specified.

36. (Previously Presented) The method of claim 1, wherein the one or more pipeline locations are automatically specified.

37. (Previously Presented) The method of claim 1, wherein the clocked elements comprise flip-flops.

38. (Previously Presented) The method of claim 1, wherein the clock element modification comprises inserting at least one clock element at the one or more pipeline locations.

39. (Previously Presented) The method of claim 6, wherein the one or more parameters comprises an operating frequency and an efficiency per cycle.

40. (Previously Presented) The method of claim 6, further comprising examining the effects on the one or more parameters, wherein the clock element modification and parameter effect examination is iteratively performed.

41. (Previously Presented) The method of claim 7, further comprising examining effects of the clock element modification and placement location as a mixed programming problem.

42. (Previously Presented) The apparatus of claim 12, wherein the design comprises a central processing unit (CPU) in which the one or more pipeline locations are specified.

43. (Previously Presented) The apparatus of claim 12, wherein the clock element modification means comprises a computer processor.

44. (Previously Presented) The apparatus of claim 12, wherein the clocked elements comprise flip-flops.

45. (Previously Presented) The apparatus of claim 12, wherein the clock element modification comprises means for inserting at least one clock element at the one or more pipeline locations.

46. (Previously Presented) The apparatus of claim 17, wherein the one or more parameters comprises an operating frequency and an efficiency per cycle.

47. (Previously Presented) The apparatus of claim 17, further comprising means for examining the effects on the one or more parameters, wherein the clock element modification and parameter effect examination is iteratively performed.

48. (Previously Presented) The apparatus of claim 18, wherein the clocked element modification means and placement location means comprise the same device.

49. (Previously Presented) The apparatus of claim 18, further comprising means for examining effects of the clock element modification and placement location as a mixed programming problem.

50. (Previously Presented) The article of manufacture of claim 23, wherein the design comprises a central processing unit (CPU) in which the one or more pipeline locations are specified.

51. (Previously Presented) The article of manufacture of claim 23, further comprising an input for receiving the one or more pipeline locations input by a user.

52. (Previously Presented) The article of manufacture of claim 23, wherein the method further comprises specifying the one or more pipeline locations.

53. (Previously Presented) The article of manufacture of claim 23, wherein the clocked elements comprise flip-flops.

54. (Previously Presented) The article of manufacture of claim 23, wherein the clock element modification comprises inserting at least one clock element at the one or more pipeline locations.

55. (Previously Presented) The article of manufacture of claim 28, wherein the one or more parameters comprises an operating frequency and an efficiency per cycle.

56. (Previously Presented) The article of manufacture of claim 28, wherein the method further comprises examining the effects on the one or more parameters, wherein the clock element modification and parameter effect examination is iteratively performed.

57. (Previously Presented) The article of manufacture of claim 29, wherein the method further comprises examining effects of the clock element modification and placement location as a mixed programming problem.

58. (Previously Presented) The method of claim 1 which is performed within an electronic design tool.

59. (Previously Presented) The apparatus of claim 12 in which the apparatus comprises an electronic design tool.

60. (Previously Presented) The apparatus of claim 59 in which the electronic design tool comprises a layout tool.